EPFL

Patterning at nanoscale: mCP, NIL and stenciling

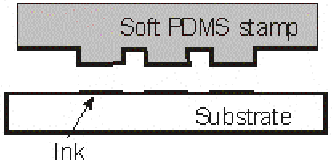
Micro-530

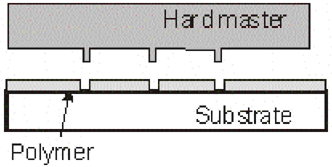
École polytechnique fédérale de Lausanne

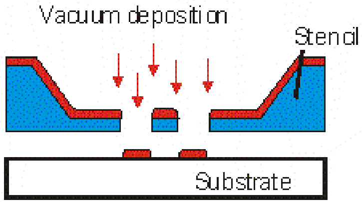
Emerging Nanopatterning Methods

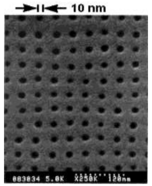
(Replication)

Soft-lithography	Nanoimprint lithography	Nanostencil lithography
Ink delivery molecules, wet *soft-contact*	Thermo-mechanical, nano-imprinting, *hard contact*	Local deposition stencil, vacuum *no contact*

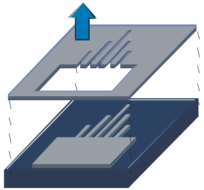




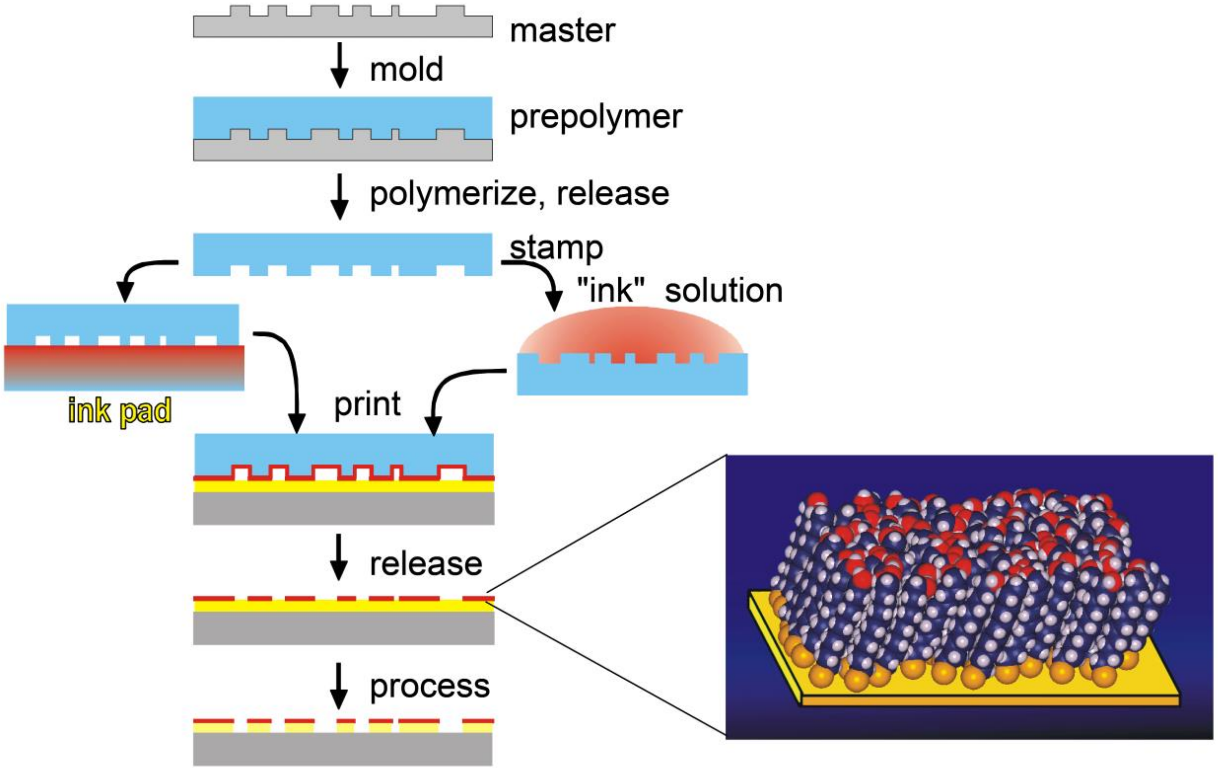




10 nm
Candidate for
Integrated Circuit



Microcontact Printing (μCP)



Microcontact Printing

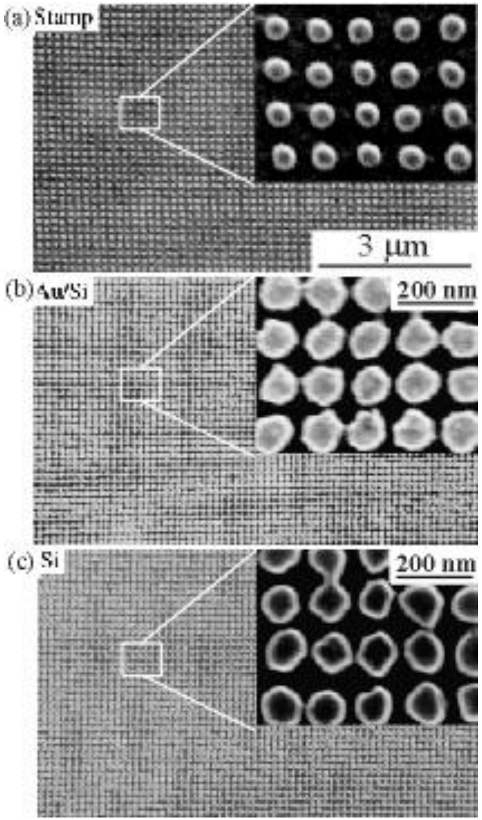
High-resolution µCP:

a) Scanning electron micrograph of a stamp with 60 nm dots.

b) The corresponding gold dots fabricated by printing and etching were slightly broadened due to ink diffusion and substrate roughness.

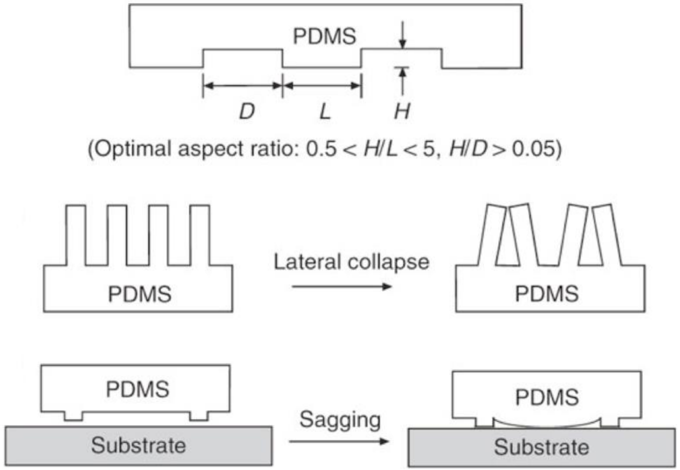
c) The gold pattern served as a mask to etch the bare regions 250 nm deep into the underlying silicon by reactive ion etching.

http://zurich.ibm.com



Microcontact Printing

- Possible problems and limitations
- Aspect ratio of stamp features
- Lateral collapse
- Sagging



Microcontact Printing

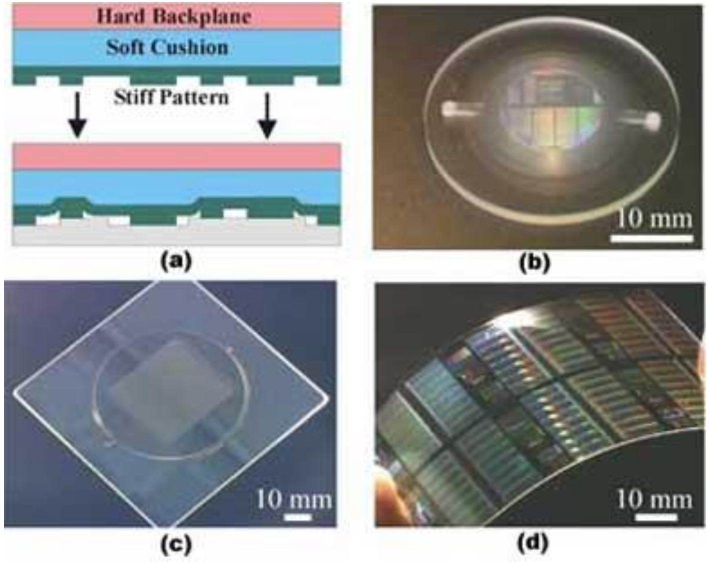
Examples of layered hybrid stamps:

a) Scheme of trilayer stamp (hard backplane, elastomeric cushion, hard polymer) showing improved adaptation to an uneven substrate

b) Trilayer stamp with 270 nm features

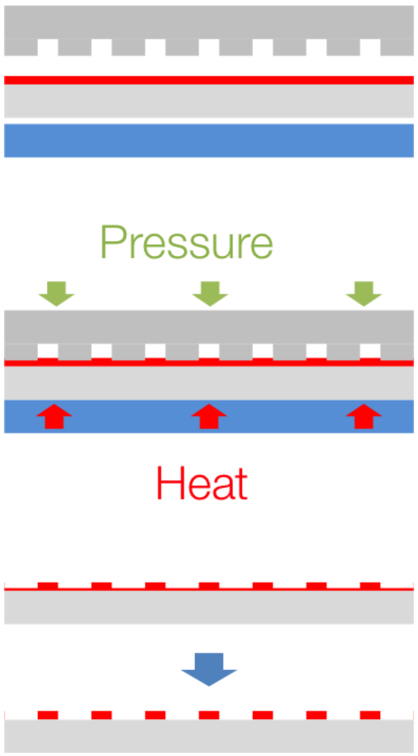
c) Bilayer stamp with 5 µm features on a 125 mm glass plate

d) Example of a two layer, thin film stamp composed of a 100 µm glass backplane and a 30 µm polymer film with 270 nm features.



[From B. Michel, H. Schmid, Macromolecules 33 (2000) 3042].

Nano-Imprint Lithography



Imprint stack preparation

Stamp (or mold), Resist, Substrate, Chuck

Imprinting

Pressure / temperature / time profile

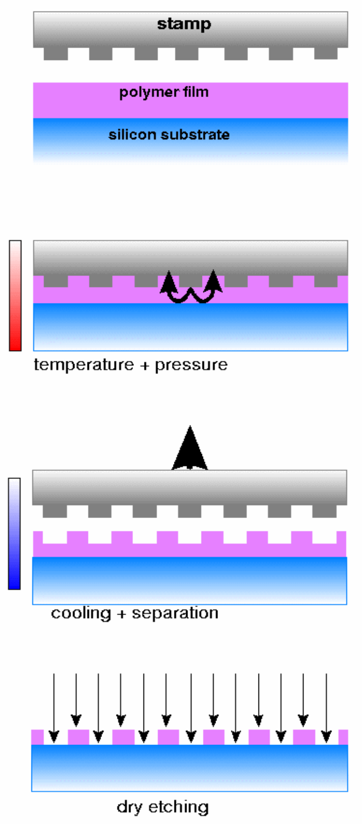
Separation

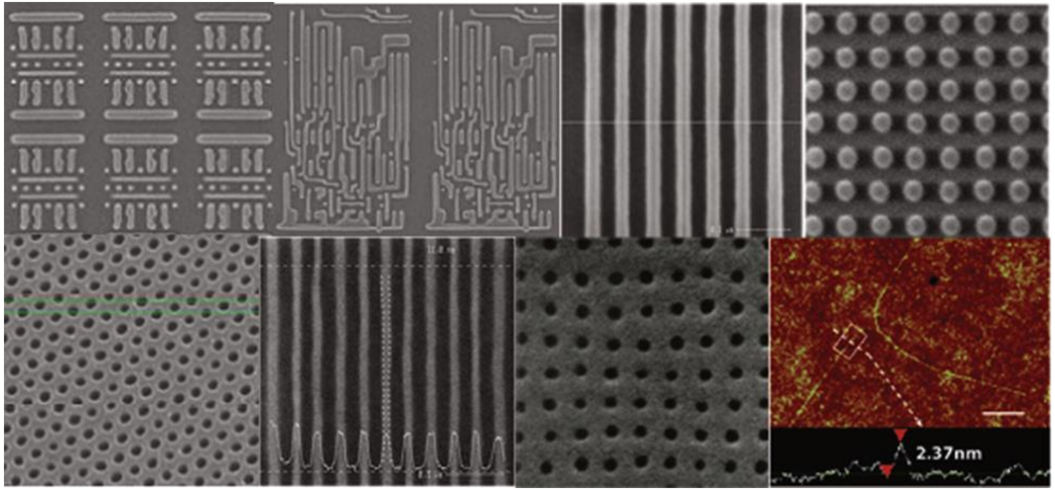
Temp control

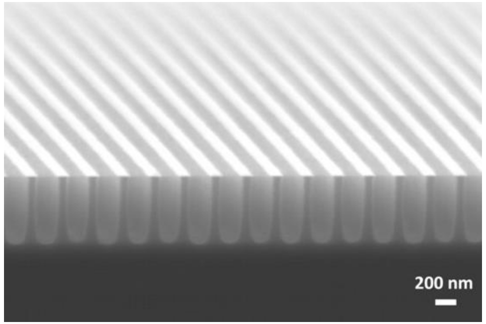
Residual layer etch

Remove thin resist layer by O2 plasma

Nano-Imprint Lithography

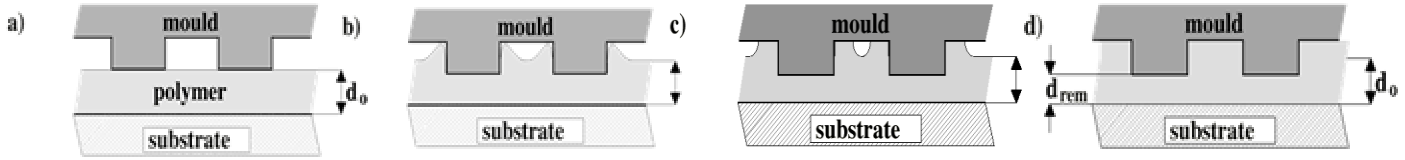


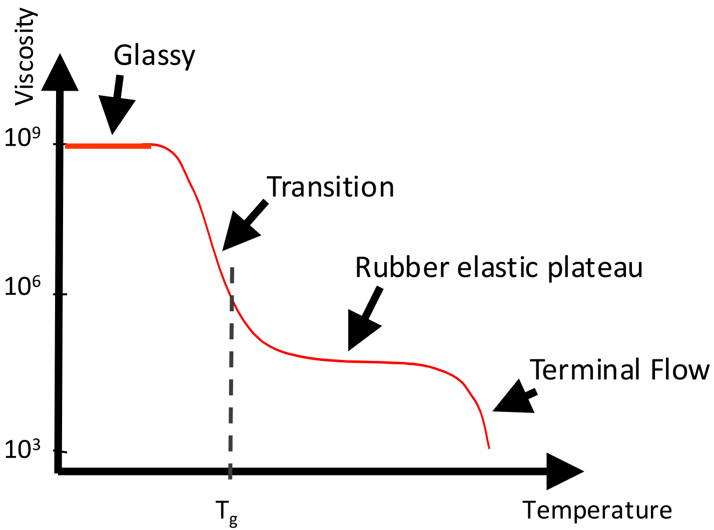


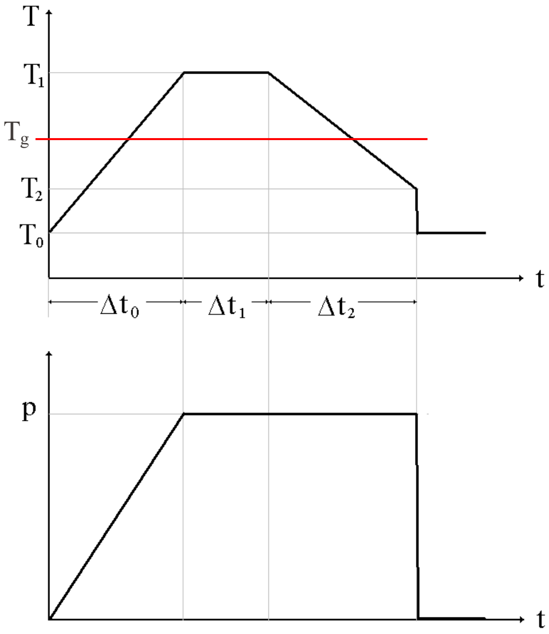


S. Chou et al. *Science 5 April 1996: Vol. 272 no. 5258 pp. 85-87*

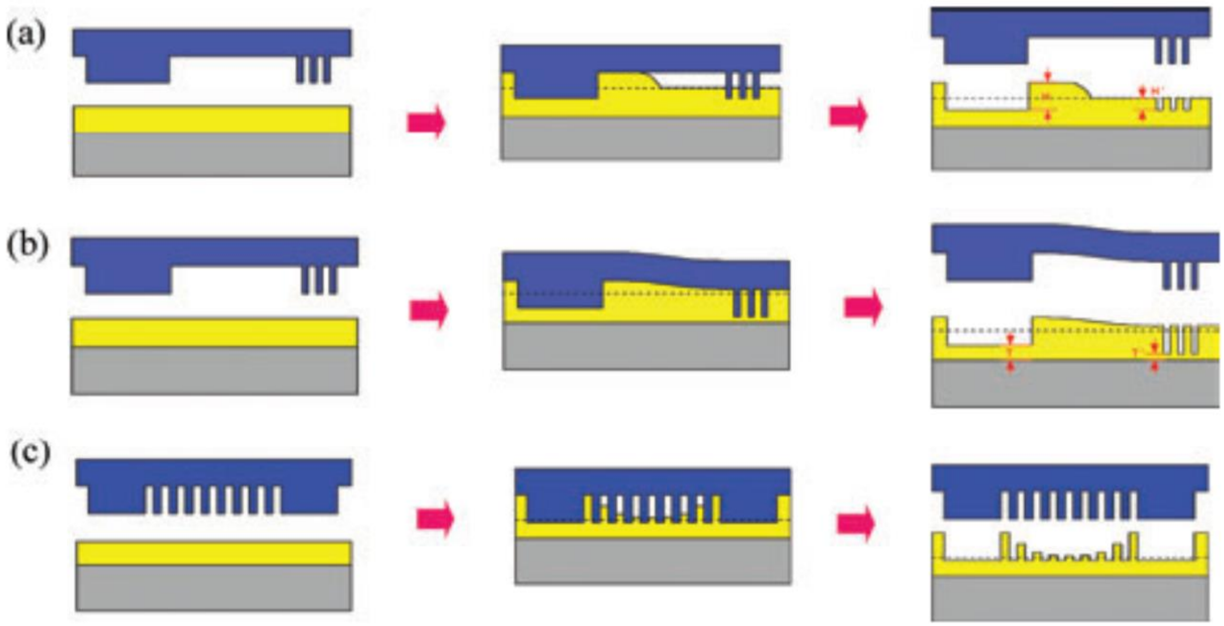
Nanoimprint Process Model







Issues with thermal NIL

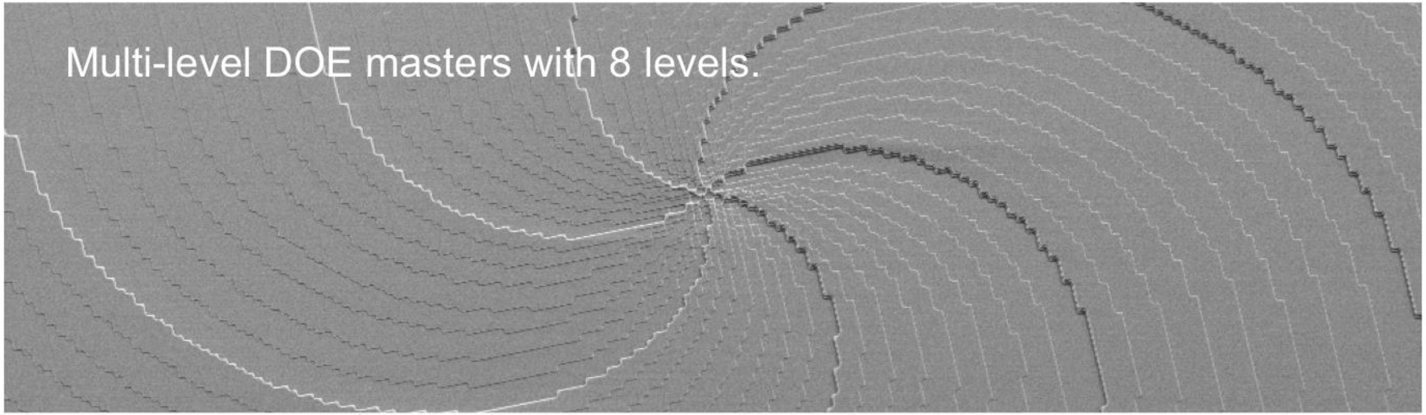


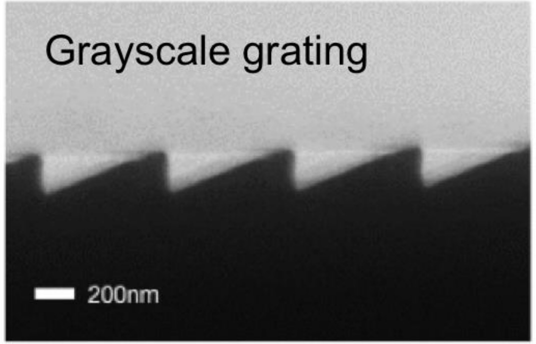
NIL examples

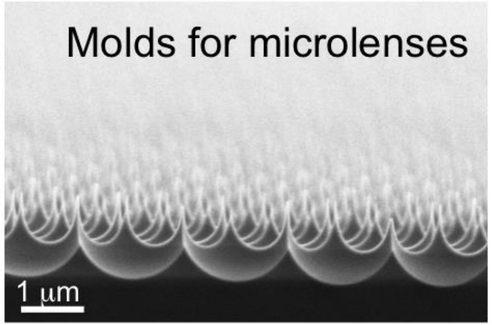
- Master stamp is costly
- Replicate master in working stamp
- Use working stamp for substrate imprinting and for mass fabrication
- Working stamp can be Nickel, Polymer, etc.

https://www.nilt.com/

NIL examples

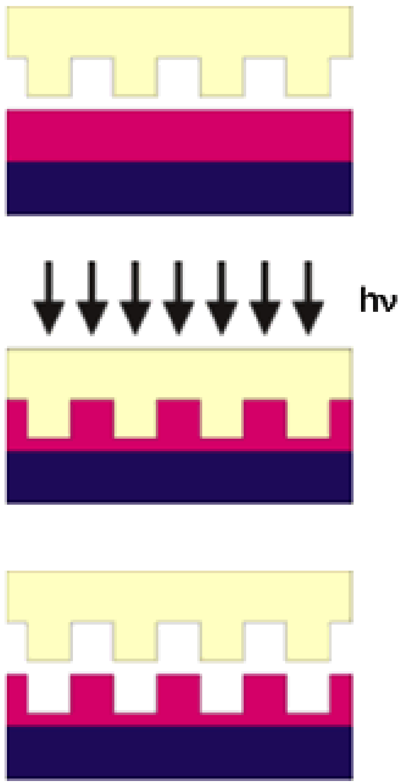




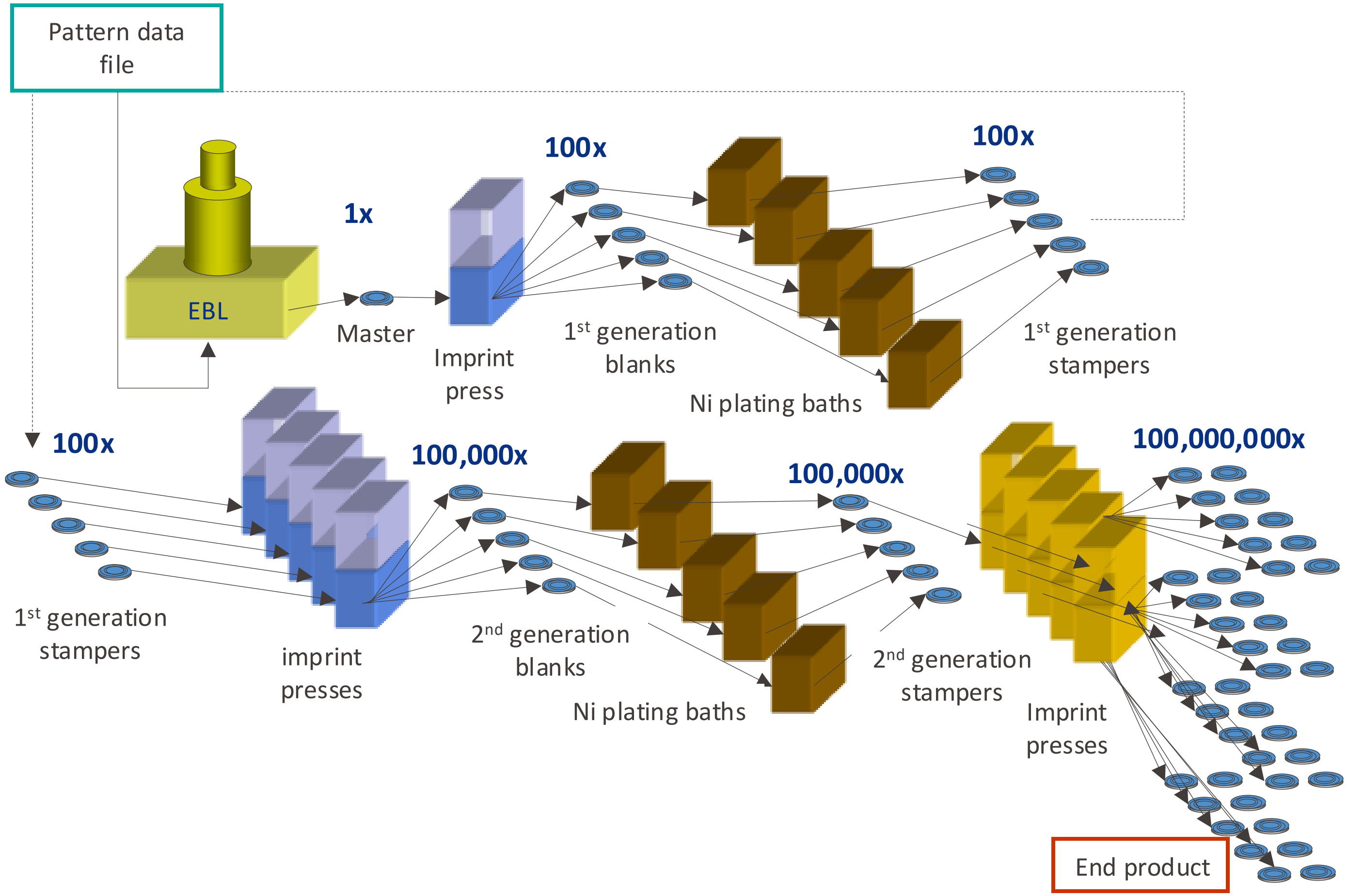


UV-NIL

- UV nanoimprint based on liquid polymer

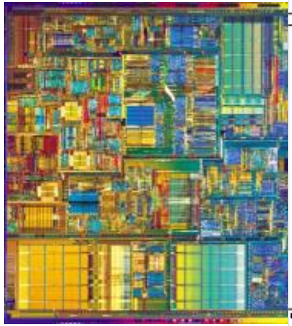


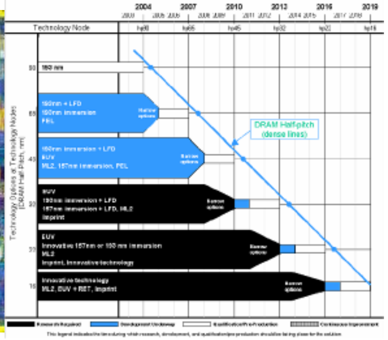
NIL in Mass Production



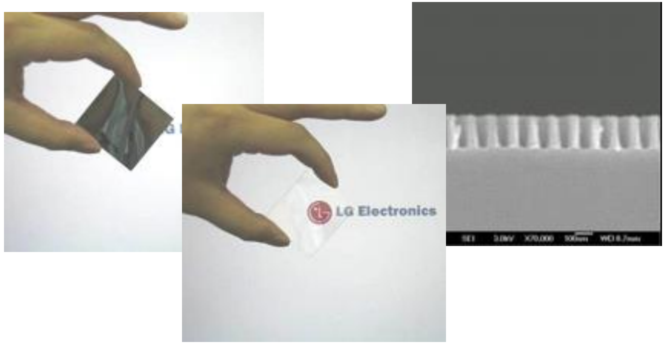
Nanopatterning – Main NIL Applications

High End Microelectronic Chips

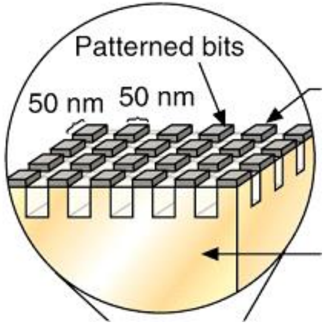


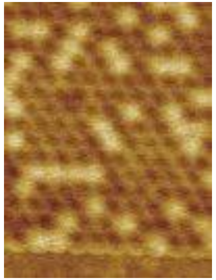


Wire Grid Polarizer

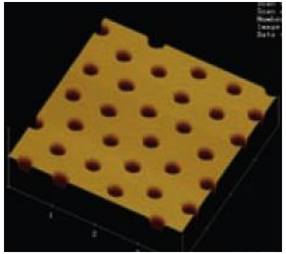


Patterned Magnetic Media

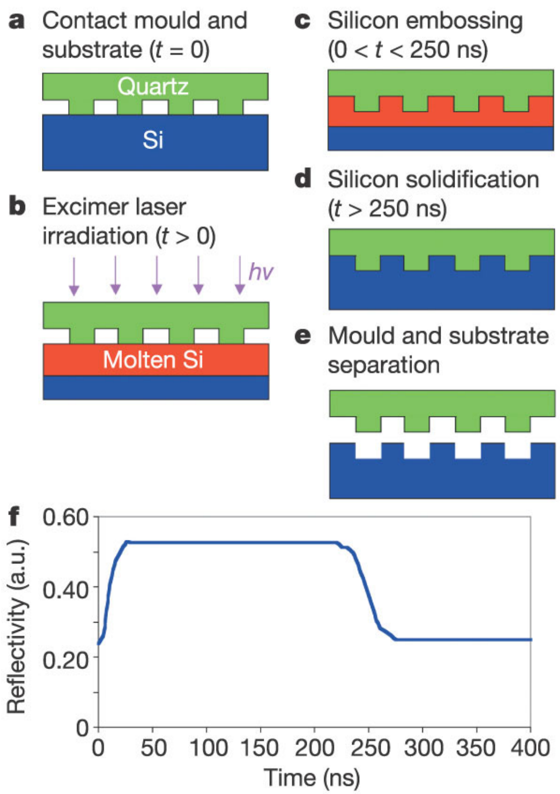


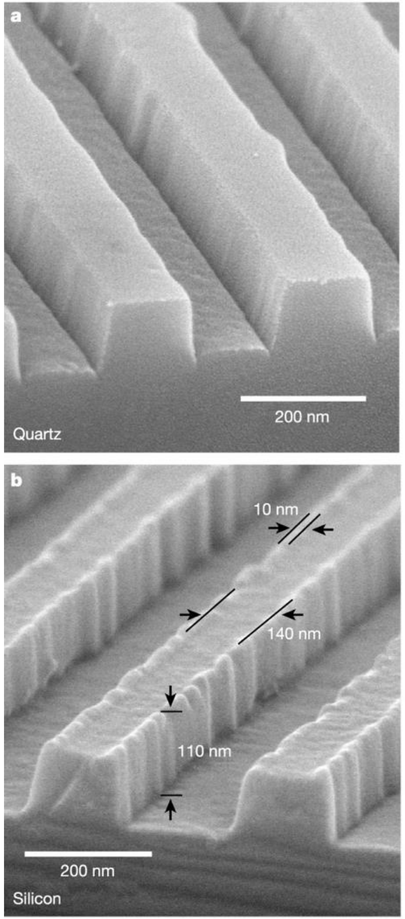


High Brightness LEDs



Direct printing into silicon





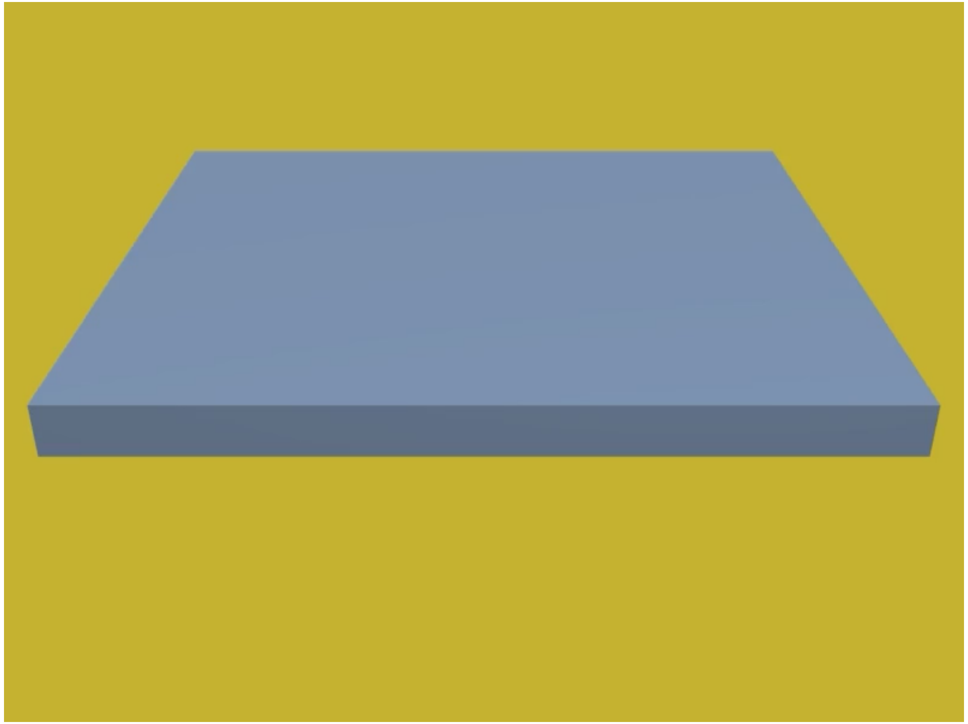
Stephen Y. Chou, Chris Keimel and Jian Gul Nature 417, 835-837(20 June 2002)

Patterning at nanoscale: Nanostencil Lithography

Micro-530

École polytechnique fédérale de Lausanne

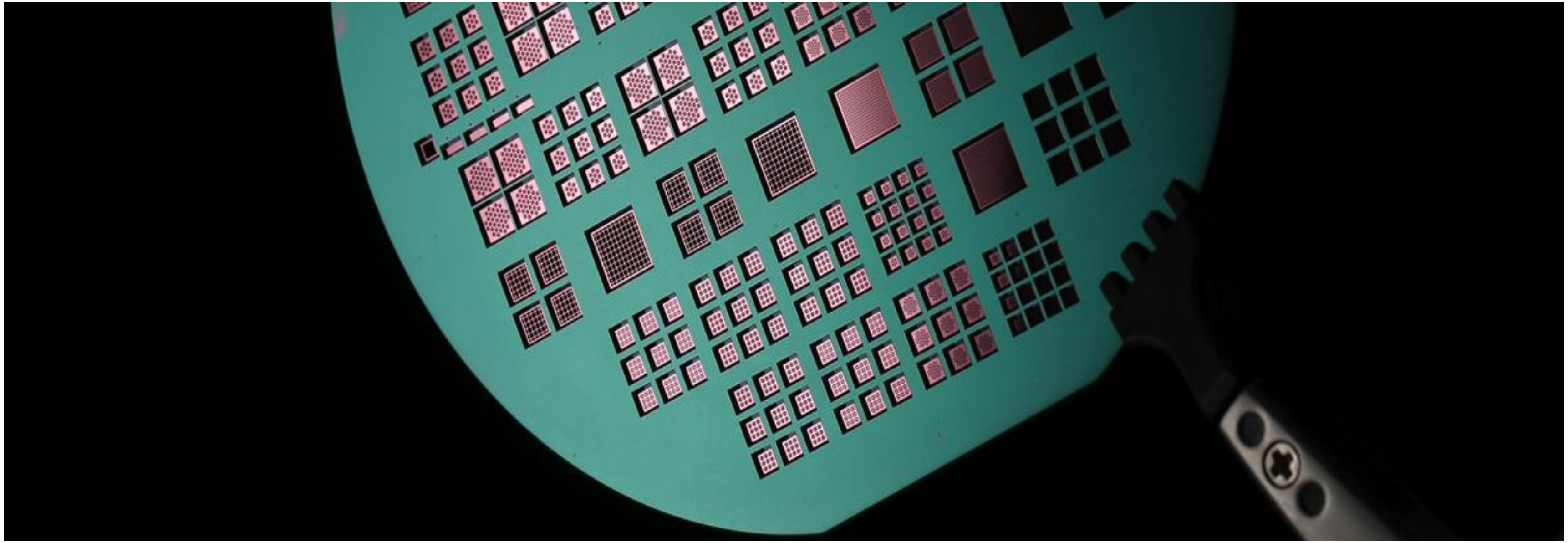
Stencil lithography (cartoon)



- Patterning without photoresist
- Very small (<100nm)
- Very large (mm)
- Vacuum clean

- Deposition
- Etching
- Implantation

Nanostencil



Challenges:

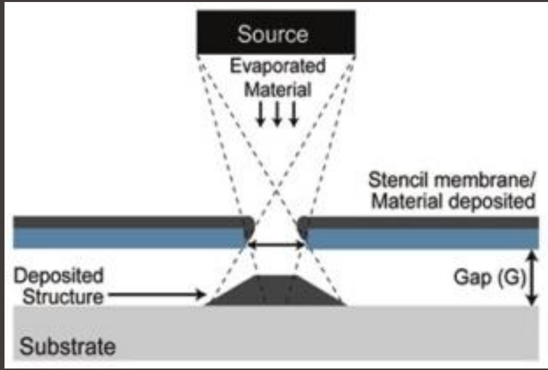
- Gap
- Blurring
- Membrane stability
- Alignment

Opportunities:

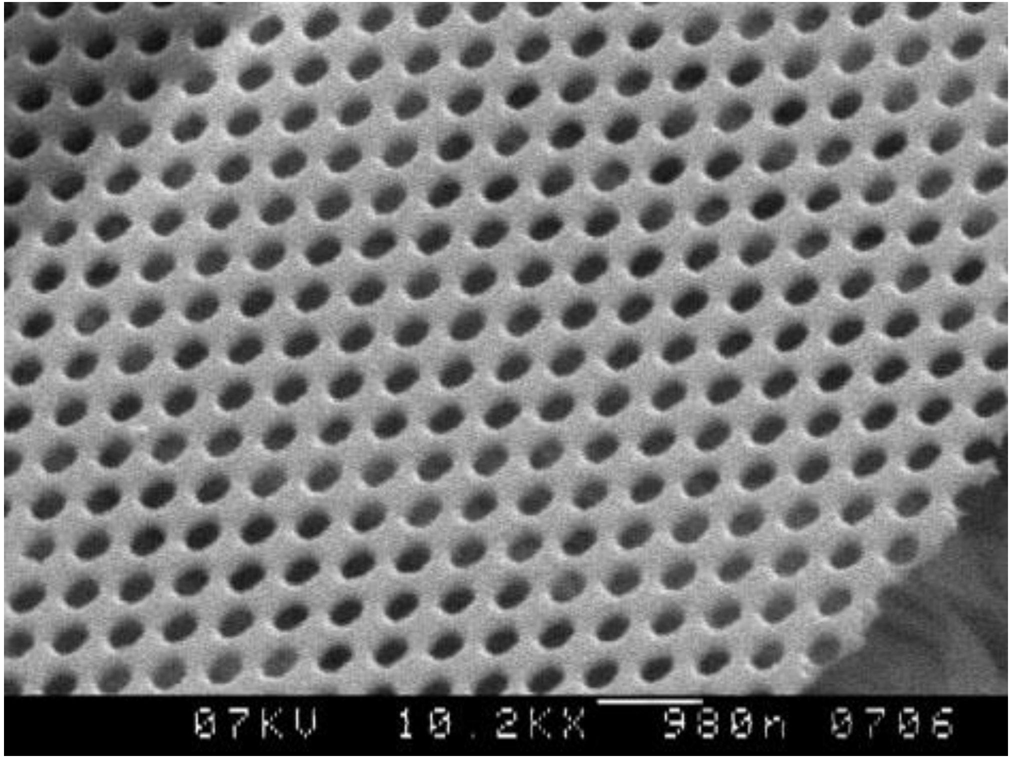
- Vacuum clean
- No resist chemistry
- Fast and simple
- Cost efficient nanofabrication
- Wide choice of material & substrates
- Mainly for PVD, but also ion implantation and dry etching

What are the challenges?

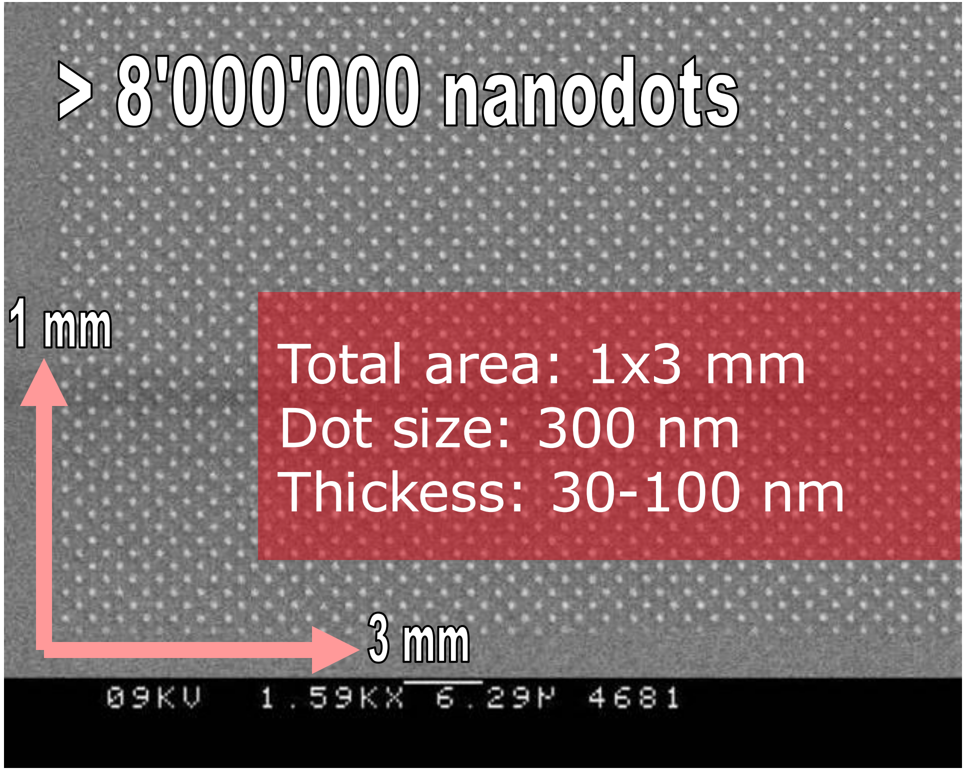
What are the opportunities?

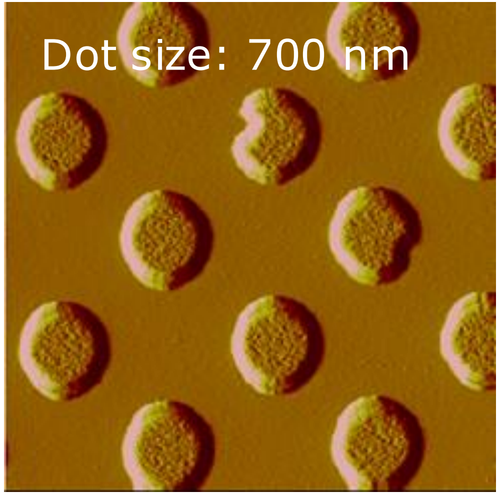


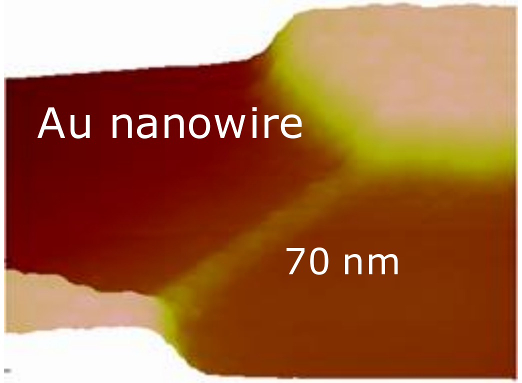
Nanosieves as stencils



Scalable nanostencil
... large membranes







Microelectronic Engineering 53 (2000) 403-405

Stencil fabrication

LPCVD 50-500 nm thick SiN

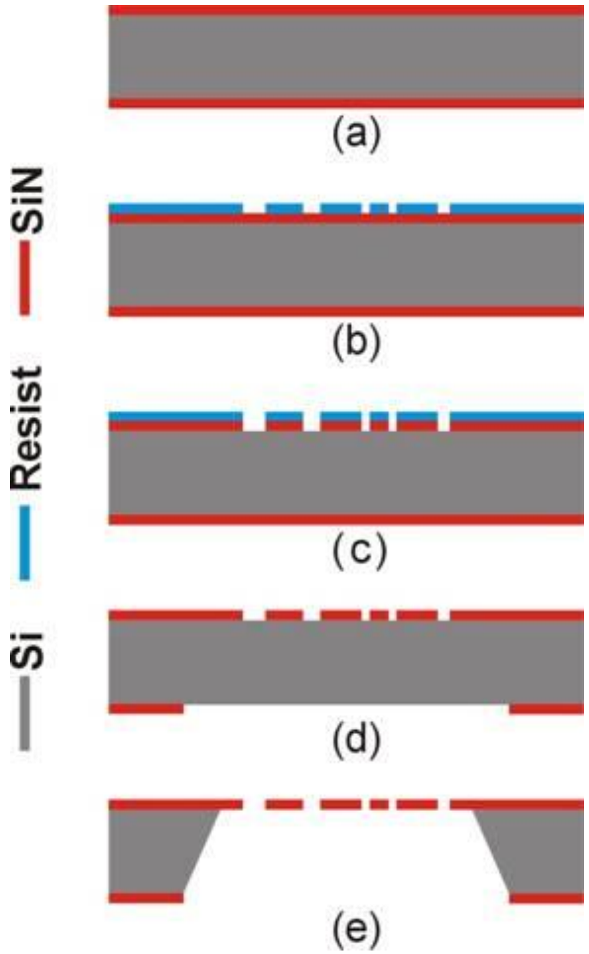
Pattern definition in photoresist

Pattern transfer into SiN

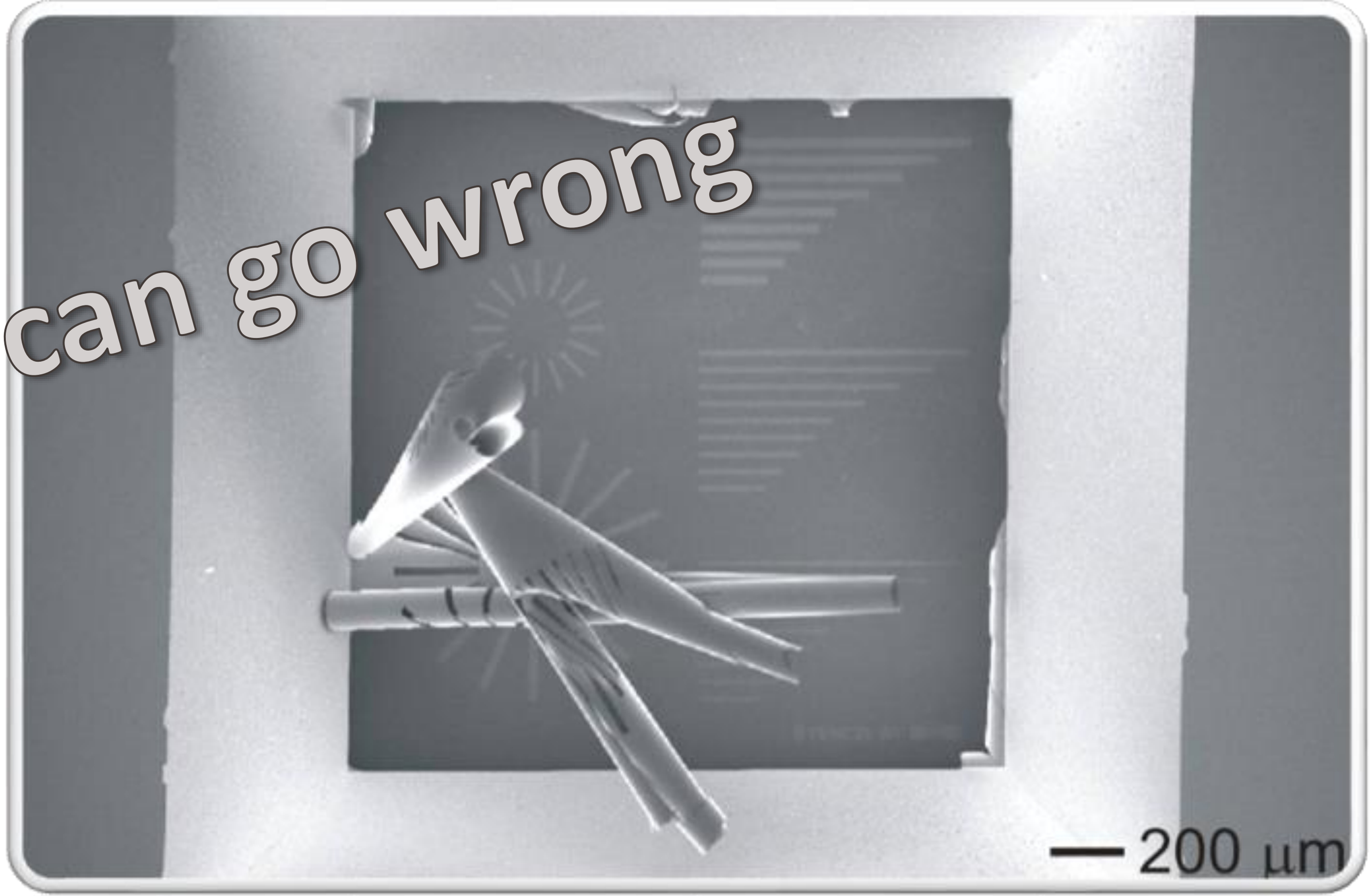
Membrane window definition and KOH etching

Fabrication of nanoscale apertures in membrane by:

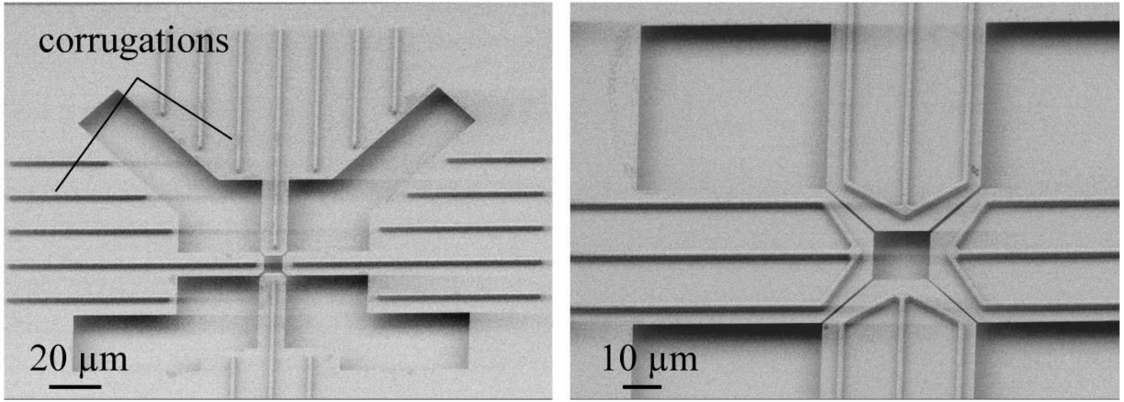
- Focused Ion Beam Milling
- Electron beam lithography
- Laser interference lithography
- Nanoimprint lithography
- Deep UV lithography



It can go wrong

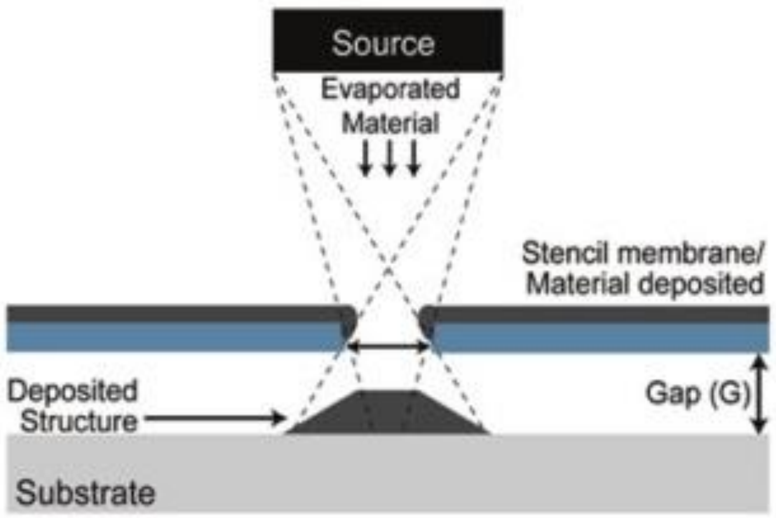


Increase moment of inertia to stabilize thin membranes

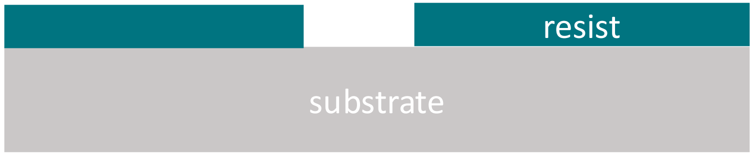


- Van den Boogaart et al. 2008

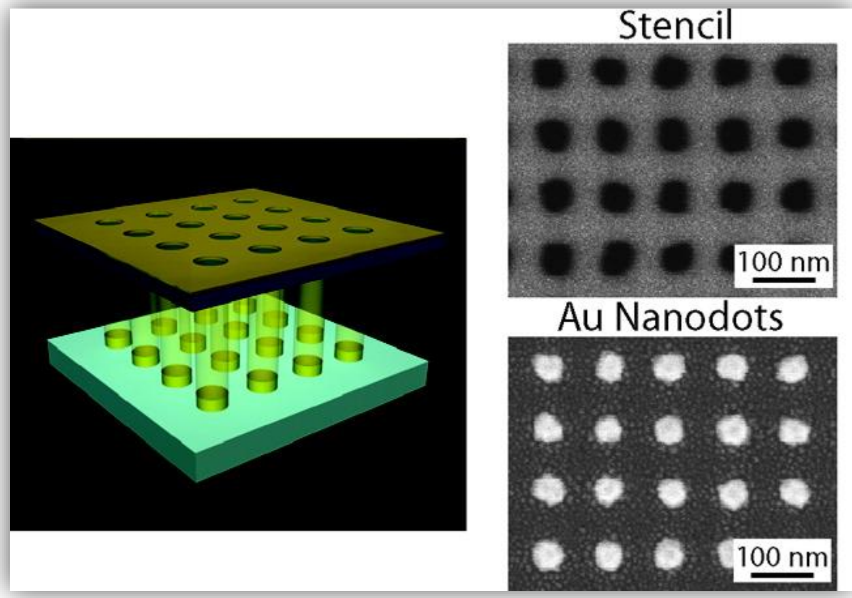
Challenge: Gap between stencil and substrate



Compare it to **Lift off:** resist is in contact with substrate; no lateral diffusion

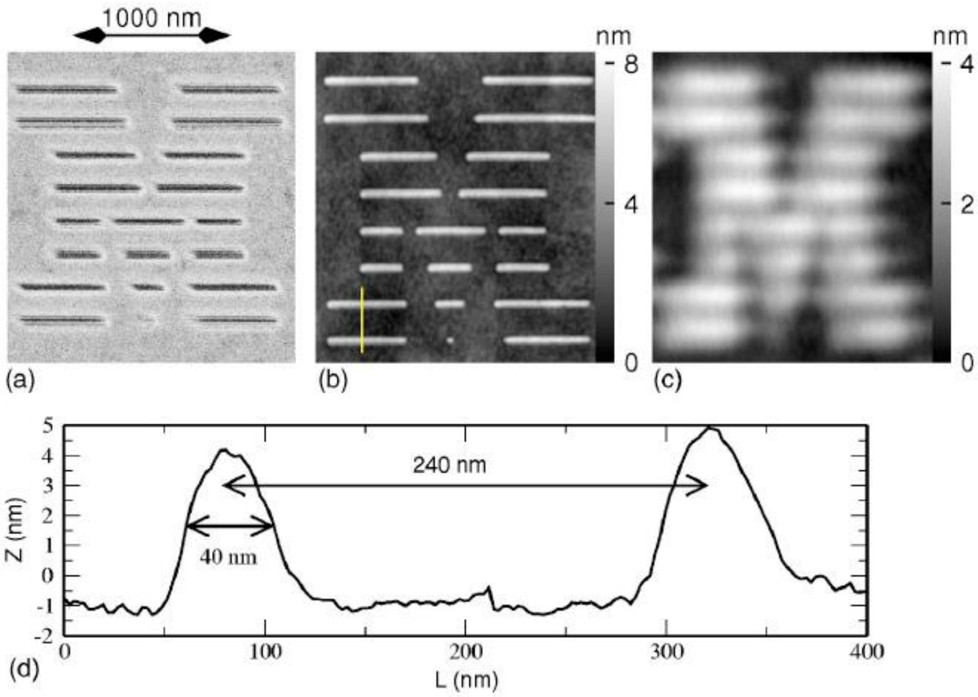


Blurring of pattern

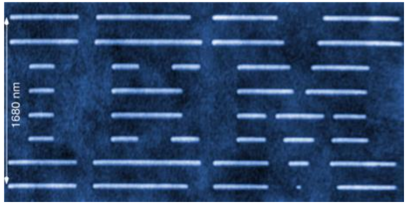


5 nm Ti / 50 nm Au
On Si/SiO2

Watch out for surface diffusion



- (a) FIB image of the stencil mask used here
- (b) DFM image of the 40 nm wide Cu structure on SiO2
- (c) DFM image of the C60 structure (diffusion induced halo).
- (d) Line profile of the section marked.



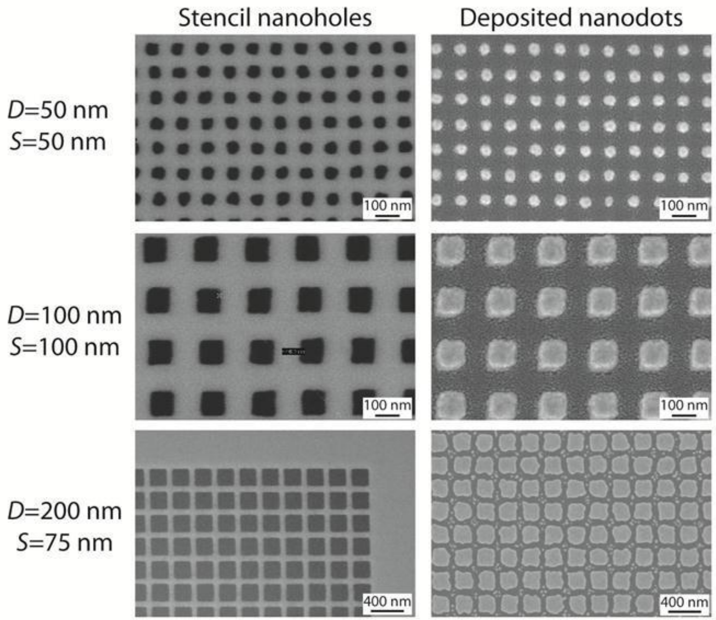
Percy Zahl et al., Rev. Sci. Instrum. 76, (2005)

IBM Research Laboratory Ruschlikon

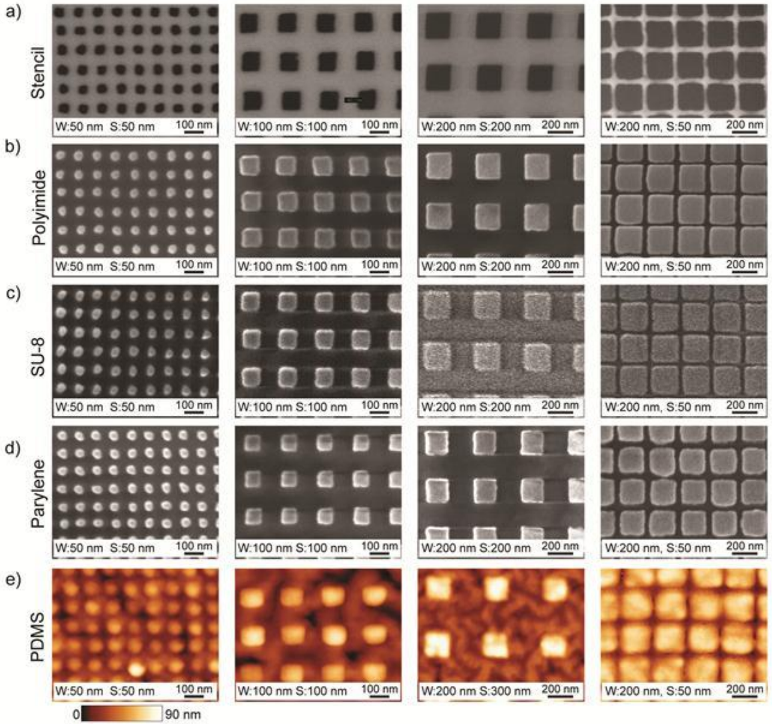
Metallic nanostructures stenciled onto …

5 nm Ti / 50 nm Au

… silicon (Au clusters)



… polymer (no Au clusters)

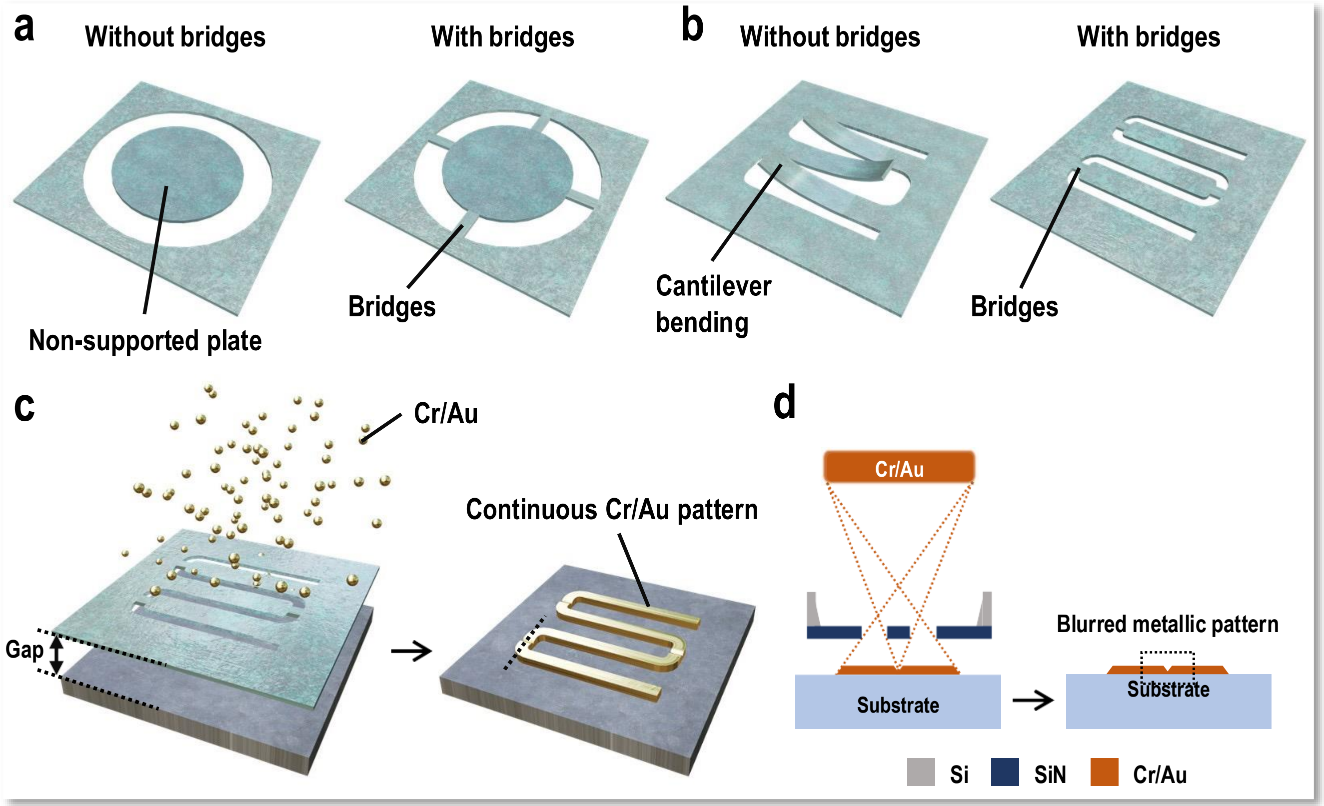


- Vazquez-Mena et al, ACS Nano (2010); ASC Nano (2012)

EPFL

STENCIL
0123456789

Bridge stencils (micro)



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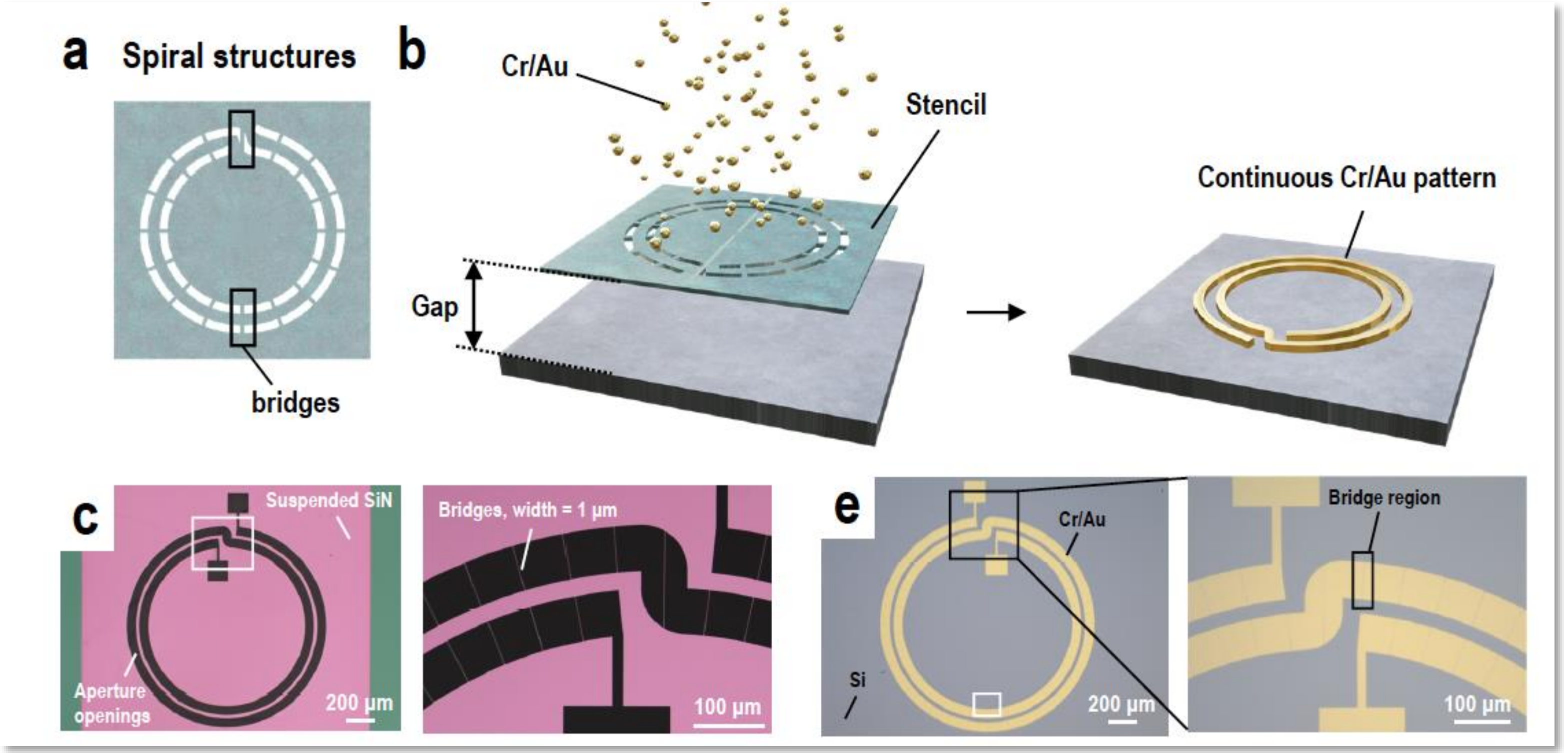
Y.C.Sun et al. *Advanced Materials Technologies (2022)*

Split ring resonator on flexible substrate



Y.C.Sun et al. *Advanced Materials Technologies (2022)*

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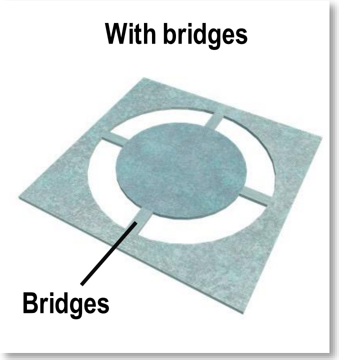

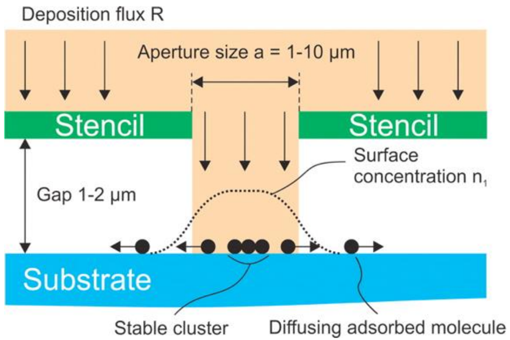

Nano stencil lithography
Take home message

Fast, parallel, scalable patterning without any wet stuff

Vacuum clean interfaces

Limits and remedies

Opportunities

Compare the different stencil applications